28.9 A 20Gb/s 1:4 DEMUX without Inductors in 0.13μm CMOS

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In recent years, high-speed communication systems beyond 10Gb/s have been realized in CMOS technology. A 40Gb/s transmitter including the MUX has been developed in 0.13μm CMOS [1], and a 40Gb/s MUX/DEMUX in 90nm CMOS has been reported [2]. These circuits extend the bandwidth with inductive peaking for 40Gb/s operation. They use supply voltages that exceed the logic supplies used in these technologies. In this paper, a 20Gb/s 1:4 DEMUX in 0.13μm CMOS is presented. This design uses no inductive peaking, which reduces area, and a 1.2V logic supply, which reduces power consumption. A coupled-latch and buffer insertion scheme increases the signal bandwidth at the 20Gb/s data rate. A divide-by-2 circuit uses a DLL to align the clock output of the frequency divider with the data center of the 1:2 DEMUX output. This design reduces the power consumption of the power-hungry divider and improves the timing margin.

Figure 28.9.1 describes the structure of the proposed 1:2 DEMUX. The 1:2 DEMUX has three stages. In one stage, two latches are coupled with shared current sources. The I_{read} and I_{hold} are equal to $I_o + \alpha$ and $I_o - \alpha$, respectively. This design is similar to the asymmetrical latch in [3]. However, the proposed coupled latch saves current in the hold mode because it fully steers the current. Furthermore, the sizing of transistors in the read and hold parts is simple. The different allocation of I_{read} and I_{hold} improves the operation speed in read mode, and the latch has less delay. However, the reduced output swing in hold mode may degrade the operating speed of the latch in the next stage. The buffer is inserted to enhance the bandwidth of the latch output. The input-to-output latency of a stage (coupled-latch (CL) + buffer) is similar to that of a conventional latch because the coupled latch has lower delay than the conventional latch does. Although the latency of the CL+buffer is similar to that of a conventional latch, it can operate at a higher bit rate due to the decreased transition times of the buffer output. The main factor limiting the operating frequency is the input-to-output latency in the stage. The latency of the stage must be less than 50ps for correct operation at 20Gb/s. The third stage includes a dummy latch for the coupled-latch structure. The 2:4 DEMUX uses a conventional latch for low power because it it is fast enough for the 10Gb/s data rate.

Figure 28.9.2(a) shows a conventional 1:4 DEMUX. The frequency divider on the left side should have large driving capability to operate with a 10GHz input clock because it directly drives many latches in the 2:4 DEMUX. This requirement leads to large power consumption in the divider. Cascaded buffers can be used in the divider output to reduce the power consumption as shown in the right side. The divider can operate above 10GHz because of the small loading capacitance of the buffer. The signal paths for D_{even} and D_{odd} should have identical cascaded buffers to keep the timing of the input data and clock in the 2:4 DEMUX. However, when the data and the clock pass through several buffers, the timing margin between them is degraded. The proposed divide-by-2 circuit in Fig. 28.9.2(b) includes a frequency divider and DLL. The divider achieves lower power consumption at frequencies above 10GHz because of the small capacitive load. The DLL synchronizes the negative edges of CLK_{in} (10GHz) with the positive edges of CLK_{fb} (5GHz). The DLL output signal needs buffers to have a large enough driving capability. To align CLK_{out} with the center of D_{even} and D_{odd}, a buffer whose delay corresponds to the C-Q delay of the 1:2 DEMUX is added in front of the clock input of the 2:4 DEMUX. The DLL architecture is shown in Fig. 28.9.2(c). The DLL output clock is generated by phase interpolation using four phases based on the divider outputs (Q and I). The DLL uses small transistors to minimize its power consumption. As implemented, the DLL draws a total current of 2mA. Figure 28.9.3 depicts the timing diagram of the 1:4 DEMUX. The divided clock CLK_{out} is aligned with the center of D_{even} and D_{odd}, and the 2:4 DEMUX has a better timing margin.

Figure 28.9.4(a) shows the static frequency divider, which consists of coupled-latches and buffers. The graph in Fig. 28.9.4(b) shows the simulated sensitivity curves of three static dividers. Although the divider using only a CL can operate at higher frequencies, it needs a larger input swing for correct operation. The sensitivity of the divider with a CL+buffer is shifted to a slightly lower frequency than that of the conventional latch, because the conventional latch has a little lower latency than the CL+buffer does. However, the divider with a CL+buffer allows a larger output swing due to its larger bandwidth. Figure 28.9.4(c) shows the output voltage swing as a function of input frequency. The output voltage swings are simulated with a single-ended input clock voltage of $400mV_{pp}$. To ensure that the divider in the chip will operate at 10GHz, its sensitivity and output swing must be optimized in the range from 8 to 15GHz. In this frequency range, the divider based on a CL+buffer has the best simulation results. Since the divider only drives a small capacitive load as shown in Fig. 28.9.2(b), it almost achieves the sensitivity shown in Fig. 28.9.4(b). As a result, it is possible to avoid large power consumption in the divider at clock frequencies above 10GHz. The divider draws 10mA. Although the DLL and cascaded buffers consume some power, the total power consumption is remarkably reduced compared to a conventional design.

The 1:4 DEMUX IC is fabricated in 0.13μm CMOS and placed in a micro-lead-frame (MLF) package, the PCB is made with Rogers 4350B material, whose signal loss at high frequency is less than that of FR4. The prototype chip could not operate with a 1.2V supply at 20Gb/s because of the reduced bandwidth of the input buffer. Although it could achieve 20Gb/s operation from a 1.5V supply, we present the results from a 1.2V supply at 19Gb/s for low power consumption. A 19Gb/s 2^{15}-1 PRBS input data of $0.5V_{pp}$ (single-ended) and a 9.5GHz input clock of $0.5V_{pp}$ (single-ended) are applied. The eye diagram of the output data and the output clock waveform are shown in Fig. 28.9.5. The eye opening width and height are 150.1ps and 62.1mV (single-ended), respectively. A die micrograph is shown in Fig. 28.9.6. The prototype chip including the input and output buffers consumes 210mW from a 1.2V supply.

Acknowledgements:
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References:
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[2] K. Kanda et al., "40Gb/s 4:1 MUX/1:4 DEMUX in 90nm Standard CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 152-153, Feb., 2005.
[3] Y. Suzuki et al., "110Gb/s Multiplexing and Demultiplexing ICs," *IEEE ISSCC Dig. Tech. Papers*, pp. 232-233, Feb., 2004.

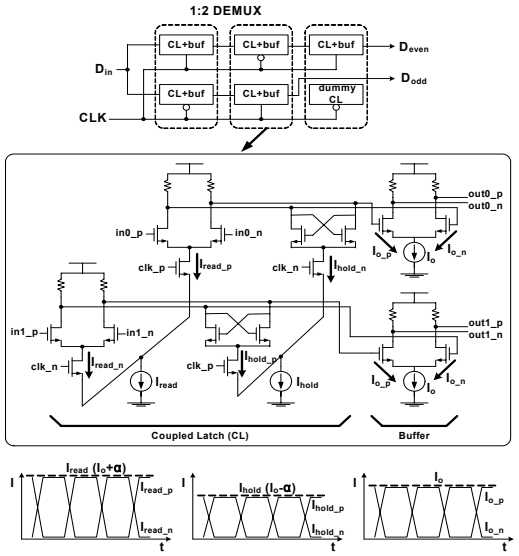


Figure 28.9.1: 1:2 DEMUX.

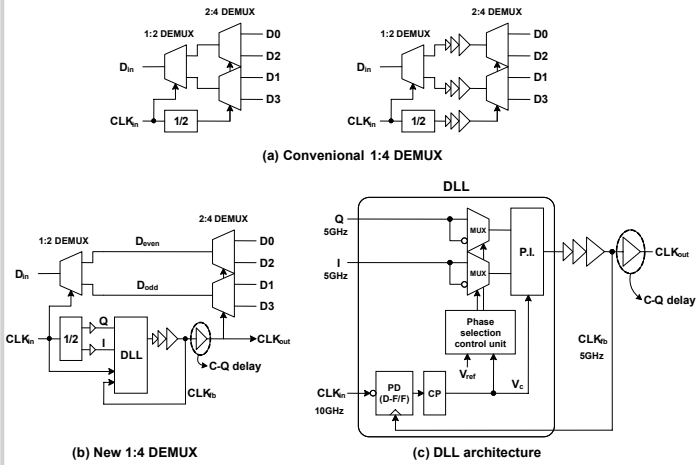


Figure 28.9.2: 1:4 DEMUX structures.

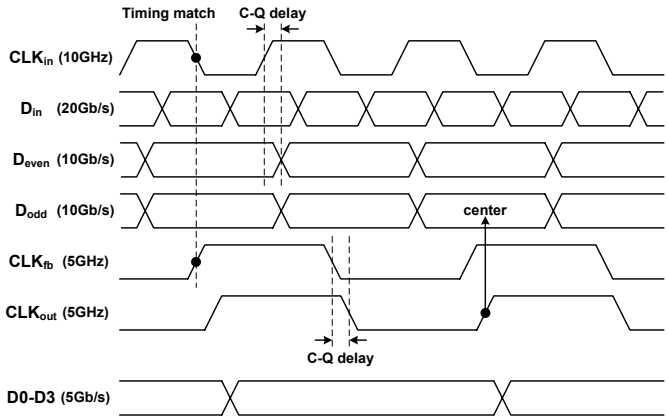


Figure 28.9.3: Timing diagram of the 1:4 DEMUX.

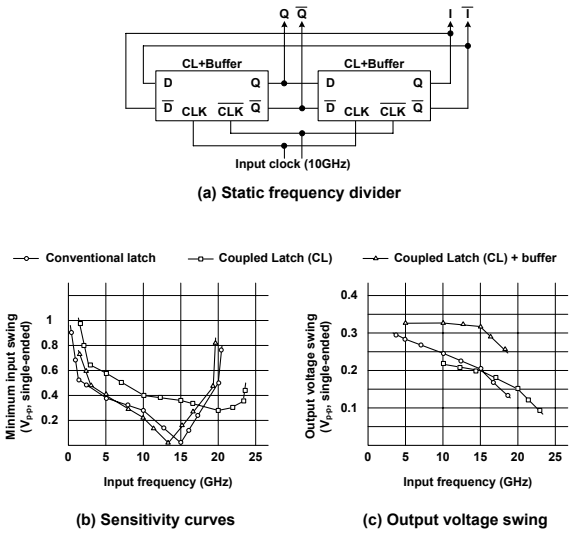
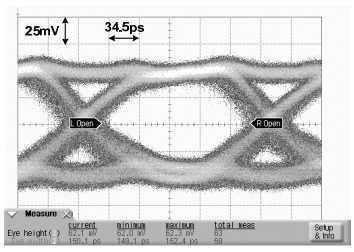


Figure 28.9.4: Static frequency divider and comparisons of three types of dividers.



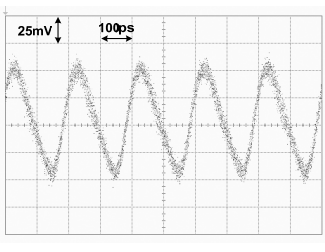
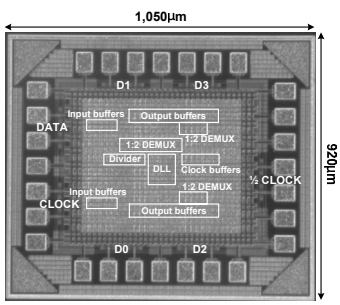


Figure 28.9.5: Output data eye diagram and divide-by-2 clock waveform.



Technology	0.13µm CMOS
Supply voltage	1.2V
Die area	1050µm× 920µm
Power consumption	210mW

Figure 28.9.6: Die micrograph.